The Design of a CMOS Nanoelectrode Array With 4096 Current-Clamp/Voltage-Clamp Amplifiers for Intracellular Recording/Stimulation of Mammalian Neurons

Jeffrey Abbott, Tianyang Ye, Keith Krenek, Ling Qin, Youbin Kim, Wenxuan Wu, *Graduate Student Member, IEEE*, Rona S. Gertner, Hongkun Park, and Donhee Ham, *Senior Member, IEEE*

***Abstract*— CMOS microelectrode arrays (MEAs) can record electrophysiological activities of a large number of neurons in parallel but only extracellularly with a low signal-to-noise ratio. Patch-clamp electrodes can perform intracellular recording with a high signal-to-noise ratio but only from a few neurons in parallel. Recently, we have developed and reported a neuro-electronic interface that combines the parallelism of the CMOS MEA and the intracellular sensitivity of the patch clamp. Here, we report the design and characterization of the CMOS integrated circuit (IC), a critical component of the neuroelectronic interface. Fabricated in 0.18-μm technology, the IC features an array of 4096 platinum black (PtB) nanoelectrodes spaced at a 20-μm pitch on its surface and contains 4096 active pixel circuits. Each active pixel circuit, consisting of a new switched-capacitor current injector—-capable of injecting from ±15 pA to ±0.7 μA with a 5-pA resolution—-and an operational amplifier, is highly configurable. When configured into the current-clamp mode, the pixel intracellularly records membrane potentials, including subthreshold activities with ∼23-μV_{rms} input-referred noise while injecting a current for simultaneous stimulation. When configured into the voltage-clamp mode, the pixel becomes a switched-capacitor transimpedance amplifier with ∼1-pA_{rms} input-referred noise and intracellularly records ion channel currents while applying a voltage for simultaneous stimulation. Such voltage-/current-clamp intracellular recording/stimulation is a feat only previously possible with the patch-clamp method. At the same time, as an array, the IC overcomes the lack of parallelism of the patch-clamp method, measuring thousands of mammalian neurons in parallel, with full-frame intracellular recording/stimulation at 9.4 kHz.**

***Index Terms*— Current clamp, extracellular recording, integrated circuits (ICs), intracellular recording, microelectrode array (MEA), nanobiointerface, nanoelectrode array, neurobiology, neurons, switched capacitor, voltage clamp.**

Manuscript received August 27, 2019; revised November 27, 2019 and March 30, 2020; accepted May 10, 2020. This article was approved by Associate Editor David Stoppa. This work was supported in part by the Samsung Advanced Institute of Technology, Samsung Electronics, under Grant A37734 and Grant A37738, in part by the Army Research Office under Grant W911NF-15-1-0565 and Grant W911NF-15-1-0548, in part by the National Science Foundation under Grant DGE1745303, in part by the National Institutes of Health under Grant 1-U01-MH105960-01, in part by the Gordon and Betty Moore Foundation, and in part by the Catalyst Foundation of Valhalla, Valhalla, NY, USA. *(Corresponding authors: Hongkun Park; Donhee Ham.)*

Jeffrey Abbott is with the John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138 USA, also with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA, and also with the Department of Physics, Harvard University, Cambridge, MA 02138 USA (e-mail: jabbott@fas.harvard.edu).

Tianyang Ye, Keith Krenek, Wenxuan Wu, and Donhee Ham are with the John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138 USA (e-mail: donhee@seas.harvard.edu).

Ling Qin was with the John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138 USA. He is now with Apple Inc., Newton, MA 02458 USA.

Youbin Kim was with the Harvard College, Harvard University, Cambridge, MA 02138 USA. He is now with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA.

Rona S. Gertner is with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA.

Hongkun Park is with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA, and also with the Department of Physics, Harvard University, Cambridge, MA 02138 USA (e-mail: hongkun_park@harvard.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.3005816

I. Introduction

CMOS microelectrode arrays (MEAs) have served as an important tool in neurobiology with their ability to record membrane potentials from a large number of neurons, with the state-of-the-art featuring as many as 10 000's of recording channels [1]–[14]. However, this neuronal recording by the CMOS MEA is an extracellular technique. The voltage it records outside the neuron is a highly attenuated and filtered version of the actual membrane potential inside the neuron, e.g., action potentials (APs) with intracellular amplitudes of ∼100 mV are attenuated to below ∼100 μV at the extracellular electrode, and their intracellular duration of ∼10 ms is reduced to as short as 100 μs at the extracellular electrode [12]. Given such a large attenuation through the extracellular neuron–microelectrode interface, the CMOS MEA cannot record small but critical synaptic events, such as postsynaptic potentials (PSPs), whose intracellular amplitudes are less than ∼5 mV. Another related drawback of the CMOS MEA is the inability for concurrent stimulation and recording of a neuron through the same electrode, as an extracellular stimulation signal needed is over $10^3\times$ larger than the extracellularly recorded signal [15].

In contrast, the patch-clamp technique, the gold standard of high-fidelity electrophysiological recording, directly accesses

the intracellular solution of a neuron with no attenuation by mechanically puncturing its membrane followed by a tight-sealing [16]. The resulting intracellular recording has a far higher sensitivity than the CMOS MEA and can routinely measure synaptic activities. This intracellular recording can be also simultaneously performed with stimulation in the form of current clamp (membrane potential recording with current injected) or voltage clamp (membrane current recording with the voltage applied). The current- and voltage-clamp modes are used for a variety of electrophysiological interrogation of neurons. For example, the current clamp recording of PSPs can find synapses, and the voltage clamp, which was used for the first measurement of currents of single ion-channel molecules [17], can characterize the effect of drugs on ion channels. This highly sensitive patch-clamp electrode, however, cannot be scaled into a dense array, such as the CMOS MEA, and only ∼10 parallel patch neuron recordings have been possible so far [18].

Recently, nanoelectrode and microelectrode of the 3-D structure were studied for the possibility of intracellular access [19]–[30]. Some of them are also scalable, defined by top–down fabrication, and so have been hoped for combining the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA. However, only a few of them [22], [23], [26], [27] could couple intracellularly with mammalian neurons and even then, only on a single or few neuron basis, and without the current-/voltage-clamp configurations, thus lacking the capability for simultaneous recording and stimulation through the same electrode.

We have very recently developed a scalable, $64 \times 64 = 4096$ platinum black (PtB) nanoelectrode array on a CMOS integrated circuit (IC), which bridges the previous gap between the intracellular sensitivity of the patch clamp and the parallelism of the CMOS MEA and performs massively parallel intracellular recording from thousands of connected mammalian neurons [31]. The CMOS IC realizes current-/voltage-clamp electronics for each of the 4096 sites or pixels. At an individual pixel, both the surface PtB nanoelectrode interfacing with a neuron and the underlying CMOS voltage/current clamp electronics operating the PtB nanoelectrode are critical for the stable intracellular recording/stimulation of the neuron. At the same time, its arrayed operation gives rise to the parallelism.

In [31], we reported network-wide intracellular recording with this chip and its application in synaptic connectivity mapping and high-throughput drug screening. This article complements [31], reporting the design of the CMOS IC, describing, in detail, how it enables the intracellular neuronal recording with simultaneous stimulation using current/voltage clamp, a feat only previously possible with the patch-clamp technique, and how it parallelizes such high-fidelity recording across the array, overcoming the limitation of the patch clamp.

Section II overviews the CMOS IC. Section III presents the pixel circuit and its current- and voltage-clamp configurations. Section IV presents the new, switched-capacitor-based current injector, a crucial pixel circuit component. Sections V and VI present electrical and electrophysiological characterizations.

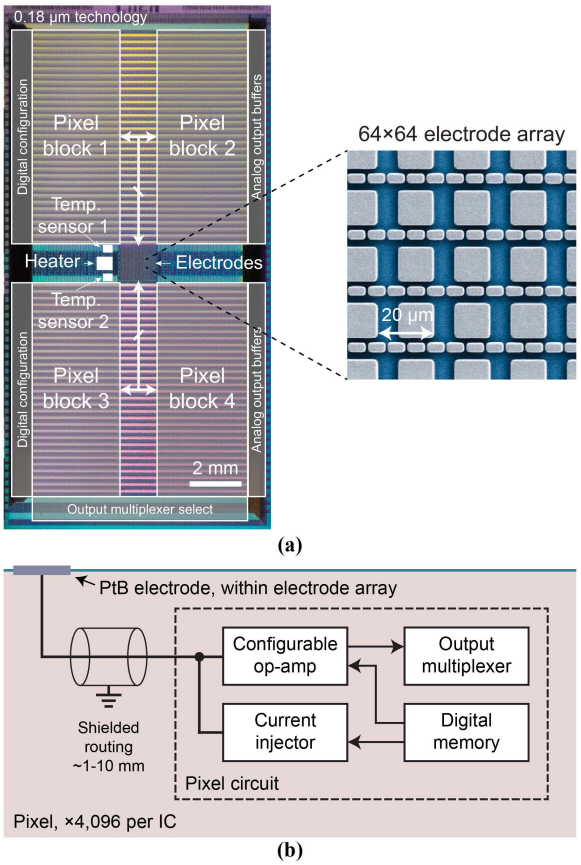


Fig. 1. (a) Chip micrograph (10×20 mm^2) along with a false-colored scanning electron microscope (SEM) image of the 4096 Al pads before post-fabrication of PtB electrodes. (b) Block diagram of an active pixel circuit.

II. Overview of the CMOS IC

Since we seek to intracellularly record and stimulate a large number of neurons, we build a dense array of electrodes capable of intracellular access with the electrode pitch comparable to mammalian neuron dimensions (20–40-μm-diameter somas) on top of a CMOS IC that integrates electronics for current- and voltage-clamp measurements at each pixel electrode. Specifically, the IC, fabricated in a dedicated 0.18-μm, one-poly, and six-metal wafer run, contains an array of 4096 surface Al pads at the chip center (pad-to-pad pitch: 20 μm), connected to 4096 active pixel circuits distributed in the four peripheral quadrants (1024 circuits per quadrant) [see Fig. 1(a)]. PtB electrodes are post-fabricated on each Al pad for intracellular access [31]. The spaces between the quadrants are used for the wiring from electrodes to pixel circuits. Each pixel circuit contains a switched-capacitor-based current injector and an op-amp [see Fig. 1(b)] to create a current- or voltage-clamp configuration (see Section III). The IC area is 10×20 mm^2. We place only one IC in each reticle occupying 20×20 mm^2 to allow a 5-mm handling area on each side of the IC for the post-fabrication of PtB electrodes. These handling areas are diced away before wire bonding and packaging [25], [31].

By separating the electrode array region in the center from the active pixel circuit region in the four peripheral quadrants, we achieve both the dense 20-μm pitch for the electrode

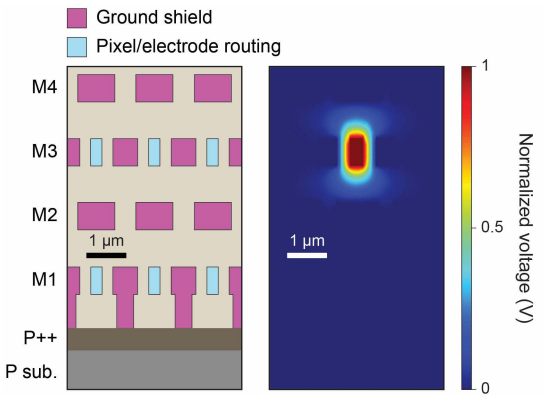


Fig. 2. Left: cross section of the densest pixel circuit to electrode routings using the bottom four metal layers; M5-M6 are used for other routings. Right: electric field simulation to calculate the routing parasitic capacitance.

array for high spatial resolution and the large 100 × 250-μm^2 area for each active pixel circuit for high configurability and low noise. This layout strategy combines the concepts of high-fidelity peripheral electronics from the switched matrix CMOS MEAs [3], [8], [11], [13] and the full-frame readout of the active-pixel sensor (APS) CMOS MEAs [1], [2], [7], [14].

The metallic routing from a pixel circuit to its electrode has a length of 1 ∼ 10 mm, depending on the location of the pixel circuit and its electrode. To mitigate the capacitive coupling between adjacent routings, we surround each routing with ground shields (Fig. 2, left). This reduces the cross-coupling capacitance to <1 fF per routing, virtually ensuring no cross-contamination between different electrode signals (see Section V-D). We minimize the parasitic capacitance $C_{p,r}$ between an individual routing and its shield by gradually increasing the spacing between them, as the density of the routings decreases further away from the electrode array. $C_{p,r}$ is ∼1-2 pF in electric field simulations (Fig. 2, right for the densest routings). The routings and shields use four of the available six metal layers and occupy ∼1.5 × 20 mm^2 in total.

To enable accurate temperature regulation, the IC contains two temperature sensors (based on the voltage differential between two diode branches of different sizes, 1:146 ratio, biased at the same current) and a heater (a 10-Ω poly-silicon resistor capable of dissipating 1.3 W) adjacent to the electrode array [see Fig. 1(a)]. They regulate the temperature of the IC to 34 °C–37 °C for cell health (see Section V-A).

The design of this IC with the particular choice of the architecture, building blocks, and target performance is guided by our goal to demonstrate the unprecedented massive parallelism in the intracellular recording of neurons. For example, we focus our design efforts significantly on realizing the front-end current-/voltage-clamp capability in each active pixel circuit, as it is essential for robust intracellular access into neurons; on the other hand, for the back-end digitization that is not fundamental to the key demonstration goal, we choose to use commercially-available high-precision analog-to-digital converters (ADCs) in order to accelerate the chip development. To drive such off-chip electronics, we implement high-speed analog multiplexers on chip. They require large bias currents to operate at frequencies in excess of 1 MHz, but, in our *in vitro* setting, the associated heat readily sinks through the open well of the solution on the chip. In fact, we actually need explicit heating of the solution to keep the cells at the temperature around 35 °C. This is in contrast to implantable applications [32], where an IC insulated by biological tissue should maintain low power density to prevent tissue damage.

III. Active Pixel Circuit

Fig. 3(a) shows the schematic of the active pixel circuit. Its main components are a switched-capacitor current injector (see Section IV) and an op-amp with configurable negative feedback networks, both of which are connected to the same PtB electrode of the pixel. It also contains a transparent latch digital memory and an output multiplexer (shared by 128 pixels per multiplexed analog output). The pixel circuit contains many transmission gate switches, controlled by the digital memory programmable in real time at up to ∼10 MHz. Many of these switches are in the op-amp negative feedback networks, making the closed-loop amplifier highly configurable. Four voltage nodes, $V_{s,1}$–$V_{s,4}$, can be connected to various voltage signals or bias references from off-chip electronics, supporting the high configurability as well as various tests. Of the pixel circuit area of 0.025 mm^2 [see Fig. 3(b)], the op-amp takes the largest part due to large transistors (Fig. 3(c), left) for minimizing noise [33]. A dedicated bias network is included for each pixel, as opposed to a global bias, to help isolate the 4096 op-amps. The current injector occupies only ∼0.003 mm^2, almost an order of magnitude smaller than standard current injectors used in MEAs [6], [9], [11], [13], attesting to the advance of our novel design (see Section IV).

For intracellular recording/stimulation, we operate the pixel circuit of Fig. 3(a) in pseudo-current- or pseudo-voltage-clamp mode (see Fig. 4), named after the similar configurations of the patch clamp. "Pseudo" emphasizes that our intracellular interface has a finite attenuation, unlike the patch clamp, as shown in the following.

A. Pseudo-Current-Clamp (pCC) Configuration

The pCC mode [see Fig. 4(a)] is obtained from Fig. 3(a) by operating the high output impedance current injector in parallel with the op-amp with the negative feedback configured as a high input impedance voltage amplifier. The current injector runs a current I_e through the electrode. This continuously injected I_e (typically on the order of −1 nA) causes and sustains the membrane permeabilization in a neuron to initiate and maintain intracellular coupling [31]. Another crucial role of this current injection is to compensate for the leakage current from within the neuron that inevitably arises due to the membrane permeabilization. At the same time, the voltage amplifier concurrently measures the electrode voltage V_e, which is an attenuated version of the membrane potential V_m. In this way, we intracellularly record membrane potentials (APs and PSPs) of the neuron. This operation is akin to the patch clamp's current-clamp recording.

The voltage amplifier is a bandpass configuration, traditionally used for low-noise neural recordings [33] [see Fig. 4(a)]. Its passband gain from V_e to the amplifier output V_{amp} is

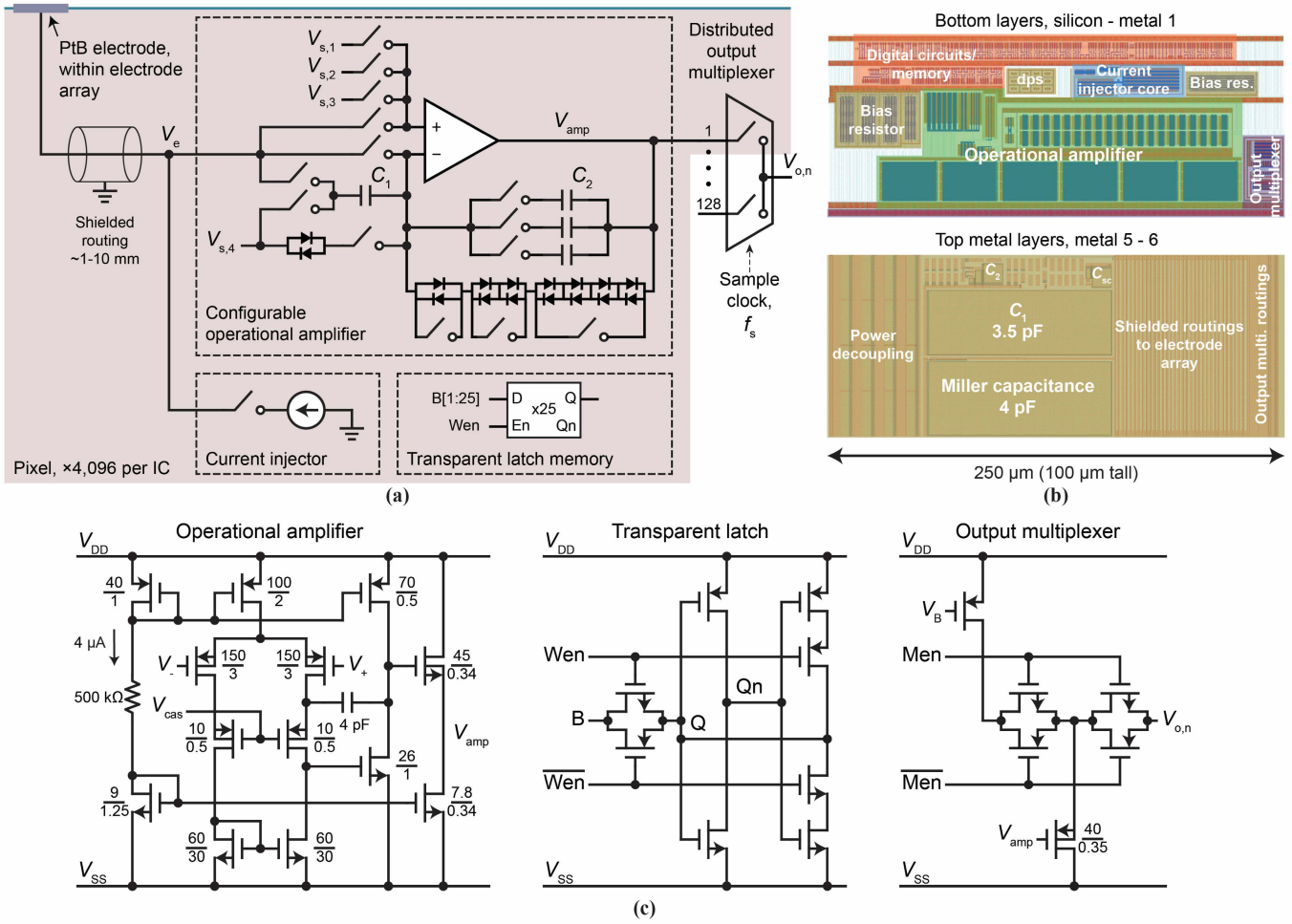


Fig. 3. (a) Active pixel circuit schematic. The switches (transmission gates) are controlled by the transparent latch memory to configure the pixel for experiments. $C_1 = 3.5$ pF; C_2 has the option of adding any of ∼5, ∼20, and ∼100 fF. (b) Active pixel circuit layout. Metal–insulator–metal capacitors are identified on the topmost metal layers. (c) Transistor-level schematics of various pixel components, in particular, op-amp (left), transparent latch (middle), and output multiplexer (right); the schematic of the current injector is shown in detail in Fig. 7.

the ratio of the feedback capacitors -C_1/C_2. This is tunable: C_1 is 3.5 pF, but C_2 can be any addition of ∼5, ∼20, and ∼100 fF [see Fig. 3(a)]. The amplifier bandwidth covers the electrophysiological spectral range: ∼1 Hz–5 kHz [34]. The low-frequency pole, $f_1 \sim 1$ Hz, is set by C_2 in parallel with the large resistance of feedback antiparallel diode pairs (dps) [options for 1–7 dps; Fig. 3(a)] biased near-zero current. The more the dps, the less the voltage drop on each dp, reducing the nonlinearity and increasing the resistance. These dps are realized using p contacts within an n-well and contain parasitic reversed biased pn diodes to the substrate and corresponding leakage currents. An additional dp tapped to $V_{s,4}$ sets a small current to tune the dc level of V_{amp} to overcome these leakage currents and to fine-tune the feedback resistance, which we discuss experimentally in Section V-C. The high-frequency pole f_2 is set by the gain-bandwidth product of the amplifier.

In the pCC recording, a change of the membrane potential V_m modulates the electrode voltage V_e according to

$$\frac{\Delta V_e}{\Delta V_m} = \frac{R_s}{R_s + R_{\text{jm}}} \frac{Z_{p,r} || Z_1}{(Z_{p,r} || Z_1) + Z_e} \approx \frac{R_s}{R_s + R_{\text{jm}}} \tag{1}$$

where R_s is the seal resistance, R_{jm} is the junctional membrane resistance, and Z_1, $Z_{p,r}$, and Z_e are the impedances of C_1, $C_{p,r}$, and the PtB electrode. The approximation in the last step of (1) is due to $|Z_e| \ll |(Z_{p,r} || Z_1)|$, which holds as the surface roughness; thus, the large surface area of the PtB electrode greatly reduces Z_e (see Section V-D). The front-end attenuation of (1) precedes the amplifier gain, contrasting the patch clamp's current clamp that has no such front-end attenuation (hence the prefix, "pseudo" in our current clamp). However, as seen shortly, this attenuation is far less than that of the extracellular recording.

For stimulation, we change I_e to modulate V_m according to

$$\frac{\Delta V_m}{\Delta I_e} \approx R_s \frac{R_m}{R_{\text{jm}} + R_m} \tag{2}$$

where R_m is the membrane resistance. Here, we have assumed $R_s \ll R_{\text{jm}} + R_m$, which holds for most nanoelectrodes (typical values: $R_s < 100$ MΩ, $R_{\text{jm}} \gg 100$ MΩ, and $R_m \sim 100$ MΩ).

Equations (1) and (2) show that a reduction of R_{jm} or an increase in R_s improves the recording amplitude and the ability to manipulate V_m for stimulation. Case in point is that the membrane permeabilization (intracellular access) induced by the aforementioned injection of I_e reduces R_{jm} to decrease the attenuation of (1) by one to two orders: APs are measured from rat neurons with ΔV_e of 1∼30 mV [31], contrasting MEA

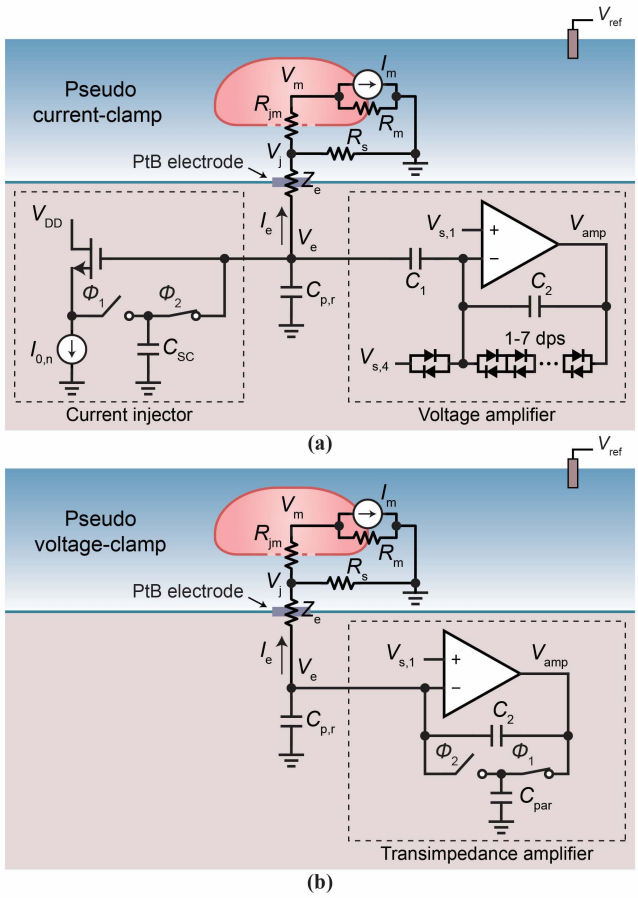


Fig. 4. (a) pCC pixel configuration. (b) pVC pixel configuration.

extracellular recording of APs in the range of 10∼100 μV. Overall, the pCC allows intracellular recording of membrane potentials of a neuron with a current injection, where the current injection can be also used for concurrent stimulation. Finally, note only a small fraction (∼1%–10%) of $I_e \sim -1$ nA enters the permeabilized neuron, as $R_s \ll R_{\rm jm} + R_m$.

Recently, a CMOS MEA [6] as well as our previous version of the CMOS nanoelectrode array [25] intracellularly recorded the membrane potential of cardiomyocytes without using the pCC but by applying a voltage to an electrode followed by a voltage recording. This voltage application also produces an electrode current to permeabilize the cell membrane for intracellular access. However, since the voltage application and voltage recording cannot be simultaneous, the electrode current is absent during the recording, and hence, the permeabilization-induced leakage from the cell cannot be compensated during the recording. This still did not prevent the intracellular recording of the membrane potentials of cardiomyocytes, as the tissue of the cardiac cells is electrically more robust due to their gap junction connections. However, this voltage-application voltage-recording approach deficient in leakage compensation cannot achieve stable intracellular recording of neuronal membrane potentials, as neurons are electrically isolated via chemical synapses and are, therefore, far more adversely affected by the leakage and the resulting depolarization.

B. Pseudo-Voltage-Clamp Configuration

The pseudo-voltage-clamp (pVC) mode [see Fig. 4(b)] is obtained by disconnecting the current injector and configuring the feedback loop of the op-amp to form a transimpedance amplifier. The feedback resistance of the transimpedance amplifier is a switched capacitor, which utilizes the switches in parallel to the feedback dps and the parasitic capacitance $C_{\rm par} \sim 35$ fF of the intermediate node between the sets of 2 and 4 dps [see Fig. 3(a)]. These switches are controlled in real time using the memory with non-overlapping clock phases Φ_1 and Φ_2. We set the effective resistance $R_{\rm TIA} = 1/f_{\rm TIA}C_{\rm par}$ of the switched capacitor typically around ∼700 MΩ using a switching frequency $f_{\rm TIA}$ of ∼ 40 kHz. The high-frequency pole of the transimpedance amplifier is set by the feedback capacitance C_2 in parallel with $R_{\rm TIA}$.

In contrast to the commonly used integrate and reset scheme, which offers the lowest noise option for current measurement [35], the feedback switched capacitor allows for sampling of all pixels via the multiplexer regardless of their sampling position as the output voltage is never completely reset. Rather, a packet of feedback charge $\Delta Q_{\rm fb} = V_{\rm amp}C_{\rm par}$ is switched from the output to the negative terminal of the amplifier to "soft-reset" the voltage across C_2, which reaches a steady state across a switching period $1/f_{\rm TIA}$ when it is equal to the transimpedance amplifier input current $I_{\rm in} = \Delta Q_{\rm fb}/f_{\rm TIA}$. The noise of this configuration is comparable to the integrate and reset scheme, as the input current is integrated across C_2 [35], except that we observe significantly more noise from pixels sampled during Φ_1 due to additional leakage current from 3 dps in parallel to the used switch [see Fig. 3(a)] (see Section V-C).

The pVC mode utilizes the transimpedance amplifier in applying a voltage $V_{s,1} = V_e$ to the electrode and simultaneously measuring the electrode current I_e. The bias point of V_e is adjusted to set the bias value of I_e at -1 nA, which induces membrane permeabilization for intracellular access. Then, the modulation of V_e is used as a voltage stimulation to induce a change of the membrane potential V_m

$$\frac{\Delta V_m}{\Delta V_e} = \frac{R_m}{R_{\rm jm} + R_m} \tag{3}$$

where we have used $|Z_e| \ll R_s$, $R_{\rm jm}$, and R_m and $R_s \ll R_{\rm jm} + R_m$. The resulting membrane current (ion channel current, such as Na^+ spikes) ΔI_m modulates the electrode current in the range of ∼100 pA–1 nA [31] according to

$$\frac{\Delta I_e}{\Delta I_m} = \frac{R_m R_s}{R_s Z_e + R_{\rm jm}(R_s + Z_e) + R_m(R_s + Z_e)} \approx \frac{R_m}{R_{\rm jm} + R_m}. \tag{4}$$

This ΔI_e is measured by the transimpedance amplifier. ΔI_e is an attenuated version of ΔI_m and contrasts the patch clamp's voltage clamp that has no such front-end attenuation (and hence the prefix "pseudo" for our voltage clamp). However, the attenuation factor is greatly reduced due to the reduction of $R_{\rm jm}$ with the intracellular access (membrane permeabilization with the injection of the bias value of I_e), just like in the pCC case. On the other hand, unlike the pCC, increasing R_s does not improve either the ability to

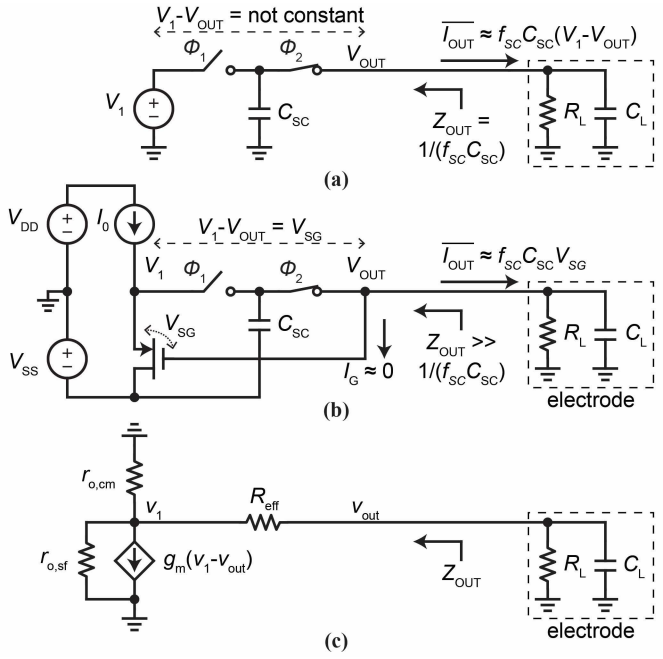


Fig. 5. (a) Switched capacitor driving an electrode. (b) and (c) Switched capacitor with an active circuit to increase output impedance and its small-signal model.

record or stimulate to the first order: as $|Z_e| \ll R_s$, $R_{\rm jm}$, and R_m, V_j is effectively connected to the pseudo-ground of the amplifier's negative terminal, which eliminates shunted membrane current through R_s. Nonetheless, a small R_s will increase the bias value of I_e for a given V_e and also decrease recording/stimulation signal transfer if $R_s \sim Z_e$.

IV. Switched-Capacitor-Based Current Injector

A key building block in the pixel circuit that enables the pCC intracellular recording is the current injector. Our novel design meets the demands of pA-range current precision needed for the membrane permeabilization, high output impedance to hold an injected current at a nearly constant and not to interfere with voltage signal amplification, and a small area such that it can be integrated into each of the 4096 pixels.

A. Basic Topology and Operating Principle

In Fig. 5(a), a capacitor $C_{\rm SC}$ switched between voltages V_1 and $V_{\rm OUT}$ ($V_1 > V_{\rm OUT}$) with non-overlapping clock phases Φ_1 and Φ_2 of frequency $f_{\rm SC}$ acts as a resistor $R_{\rm eff} = 1/f_{\rm SC}C_{\rm SC}$. The output current into $V_{\rm OUT}$, averaged over a clock period, is given by $\overline{I_{\rm OUT}} = f_{\rm SC}C_{\rm SC}(V_1 - V_{\rm OUT})$. As $f_{\rm SC}$ can be varied over many orders of magnitude, $\overline{I_{\rm OUT}}$ can assume a wide range of values, with its minimum value comfortably falling into the pA region. For example, with $C_{\rm SC} = 30$ fF, $V_1 - V_{\rm OUT} = 0.6$ V, and $f_{\rm SC}$ increasing from 1 kHz over many orders of magnitude, $\overline{I_{\rm OUT}}$ can be tuned up from 18 pA over the same orders of magnitude. If this switched capacitor drives an electrode immersed in an electrolyte modeled as a Faradaic resistor R_L in shunt with a double layer capacitor C_L [see Fig. 5(a)], the injected $\overline{I_{\rm OUT}} \approx f_{\rm SC}C_{\rm SC}(V_1 - V_{\rm OUT})$ cannot be fixed at a constant as $V_{\rm OUT}$ varies with time. The corresponding small-signal output impedance, $Z_{\rm OUT} = |\partial V_{\rm OUT}/\partial \overline{I_{\rm OUT}}|$, is $R_{\rm eff} = 1/f_{\rm SC}C_{\rm SC}$.

To increase $Z_{\rm OUT}$ substantially, we can build a source follower circuit around the switched capacitor, as shown in Fig. 5(b), to set $V_1 - V_{\rm OUT}$ at a fixed value: the V_1 and $V_{\rm OUT}$ nodes of the switched capacitor are connected to the source and gate of the PMOS transistor. V_1 then follows $V_{\rm OUT}$ to maintain $V_1 - V_{\rm OUT}$ at $V_{\rm SG}$, i.e., the source–gate voltage of the transistor. In the absence of channel length modulation, $V_{\rm SG}$ is fixed at a constant value by the bias current I_0 and independent of $V_{\rm OUT}$. In this ideal case, $\overline{I_{\rm OUT}} \approx f_{\rm SC}C_{\rm SC}(V_1 - V_{\rm OUT}) = f_{\rm SC}C_{\rm SC}V_{\rm SG}$ is perfectly independent of $V_{\rm OUT}$ and can be set by $f_{\rm SC}$ and $C_{\rm SC}$ to a constant value. Correspondingly, $Z_{\rm OUT} = \infty$. In the realistic case with the transistor channel length modulation, $V_{\rm SG}$ does vary with $V_{\rm OUT}$ but only weakly, so $\overline{I_{\rm OUT}} \approx f_{\rm SC}C_{\rm SC}(V_1 - V_{\rm OUT}) = f_{\rm SC}C_{\rm SC}V_{\rm SG}$ exhibits only a small dependence on $V_{\rm OUT}$. The corresponding $Z_{\rm OUT}$ calculated with the small-signal model of Fig. 5(c) is

$$Z_{\rm OUT} = \frac{r_{o,\rm cm}\left(R_{\rm eff} + r_{o,\rm sf}\right) + r_{o,\rm sf}R_{\rm eff}\left(1 + g_m r_{o,\rm cm}\right)}{r_{o,\rm cm} + r_{o,\rm sf}} \approx (g_m r_o/2) \times 1/(f_{\rm SC}C_{\rm SC}) + r_0/2 \quad (5)$$

where $r_{o,\rm sf}$ and $r_{o,\rm cm}$ are the output resistances of the PMOS transistor and the current (I_0) bias circuit, respectively, and g_m is the transconductance of the PMOS transistor. The second line is approximated by setting $r_{o,\rm sf} \approx r_{o,\rm cm} \equiv r_o$ without losing the essence and by using $g_m r_o \gg 1$. As seen, $Z_{\rm OUT}$ is greatly boosted from $R_{\rm eff} = 1/f_{\rm SC}C_{\rm SC}$ by a factor of $g_m r_o/2$.

B. Transient Dynamics

We now discuss the transient behavior of the switched-capacitor current injector of Fig. 5(b). During a clock phase Φ_1, $C_{\rm SC}$ is disconnected from $V_{\rm OUT}$ and connected to V_1 via the switch ON-resistance $R_{\rm SW}$ ($R_{\rm SW} \ll R_L$). Throughout this Φ_1 phase, $V_{\rm OUT}$ decays with a slow time constant of the load, $\tau_L = R_L C_L$, and V_1 follows this decay to maintain $V_1 = V_{\rm OUT} + V_{\rm SG}$ [see Fig. 6(a)]. In contrast, at the onset of the phase Φ_1, the switched-capacitor voltage $V_{\rm SC}$ makes a rapid upward transition from $V_{\rm OUT}$ to $V_1 = V_{\rm OUT} + V_{\rm SG}$ [see Fig. 6(a)], rapidly charging $C_{\rm SC}$ (time constant: $\tau_1 = R_{\rm SW}C_{\rm SC} < 1$ ns $\ll \tau_L$) with $\Delta Q_{\rm SC} = C_{\rm SC}\Delta V_{\rm SC} = C_{\rm SC}V_{\rm SG}$.

During the subsequent clock phase Φ_2, $C_{\rm SC}$ is disconnected from V_1 and connected to $V_{\rm OUT}$ via $R_{\rm SW}$. This reconfiguration rapidly redistributes the charge $\Delta Q_{\rm SC} = C_{\rm SC}V_{\rm SG}$ between $C_{\rm SC}$ and C_L with a fast time constant $\tau_2 \approx R_{\rm SW}C_L C_{\rm SC}/(C_L + C_{\rm SC}) \approx R_{\rm SW}C_{\rm SC} < 1$ ns $\ll \tau_L$, discharging $C_{\rm SC}$ (lowering $V_{\rm SC}$) and charging C_L (raising $V_{\rm OUT}$) until $V_{\rm SC} = V_{\rm OUT}$ [see Fig. 6(a)]. The resulting change of the output voltage $\Delta V_{\rm OUT}$ is

$$\Delta V_{\rm OUT} = \frac{\Delta Q_{\rm SC}}{C_{\rm SC} + C_L} = \frac{C_{\rm SC}V_{\rm SG}}{C_{\rm SC} + C_L} \approx \frac{C_{\rm SC}V_{\rm SG}}{C_L}. \quad (6)$$

These changes of $V_{\rm SC}$ and $V_{\rm OUT}$ (V_1 follows $V_{\rm OUT}$ to maintain the difference $V_{\rm SG}$) occur rapidly during the very early part of the phase Φ_2 due to the short time constant τ_2 [see Fig. 6(a)]. The charge packet injected to C_L during the charge redistribution in the early part of Φ_2 is $\Delta Q_{\rm OUT} = C_L \Delta V_{\rm OUT}$.

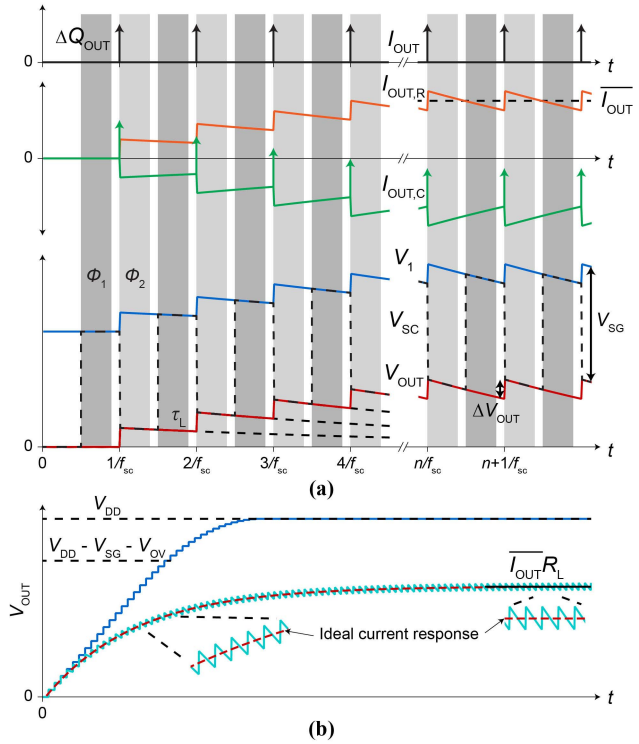


Fig. 6. (a) Timing diagram for I_{OUT}, $I_{\mathrm{OUT},R}$, and $I_{\mathrm{OUT},C}$ and V_1, V_{SC}, and V_{OUT}. (b) $V_{\mathrm{OUT}}(t)$ for the R_LC_L load (cyan, solid) in juxtaposition with $V_{\mathrm{OUT}}(t)$ for a C_L-only load (blue, solid). The response of the R_LC_L load to an ideal step current is overlaid (red, dashed) for comparison.

The output current I_{OUT} is due to this charge packet injection, and its average over a clock period is given by

$$\overline{I_{OUT}} = f_{\mathrm{SC}}\Delta Q_{\mathrm{OUT}} = f_{\mathrm{SC}}C_{\mathrm{SC}}V_{\mathrm{SG}} \times \left[\frac{C_L}{C_{\mathrm{SC}}+C_L}\right] \approx f_{\mathrm{SC}}C_{\mathrm{SC}}V_{\mathrm{SG}} \quad (7)$$

which is consistent with the calculation of Section IV-A.

With repeated clock cycles, V_{OUT} is then a sequence of a rapid ΔV_{OUT} up-step (time constant τ_2) followed by a slow decay (time constant τ_L) [see Fig. 6(a)]. If we break down I_{OUT} into current $I_{\mathrm{OUT},R}$ through R_L and current $I_{\mathrm{OUT},C}$ through C_L ($I_{\mathrm{OUT}} = I_{\mathrm{OUT},R} + I_{\mathrm{OUT},C}$) in phase Φ_2, the rapid charging of C_L in the beginning of Φ_2 is described by $I_{\mathrm{OUT}} \approx I_{\mathrm{OUT},C} > 0$, while the background slow discharging of C_L through R_L is described by $-I_{\mathrm{OUT},C} \approx I_{\mathrm{OUT},R}$ ($I_{\mathrm{OUT},C} < 0$) with $I_{\mathrm{OUT}} \approx 0$ [see Fig. 6(a)]. In the initial clock cycles, the charging of C_L by the charge packet injection $\Delta Q_{\mathrm{OUT}} = C_L\Delta V_{\mathrm{OUT}}$ per clock cycle exceeds its discharging through R_L per clock cycle, and thus, V_{OUT} overall rises, but once C_L is sufficiently charged at later clock cycles, its charging and discharging balance each other, and V_{OUT} reaches a plateau (except voltage ripples) [see Fig. 6(a), bottom, and Fig. 6(b)]. This evolution of V_{OUT} into the steady state, ignoring the ripples, can be quantified by evaluating V_{OUT} at $t = n/f_{\mathrm{SC}}$ or at the end of nth clock phase Φ_2 as follows:

$$V_{\mathrm{OUT}}(t) = \Delta V_{\mathrm{OUT}}\sum_{k=1}^{n}\exp\left(-\frac{k}{f_{\mathrm{SC}}R_LC_L}\right)\times\exp\left(-\frac{1}{2f_{\mathrm{SC}}R_LC_L}\right) \approx \overline{I_{OUT}}R_L\left[1-\exp\left(-\frac{t}{R_LC_L}\right)\right] \quad (8)$$

where we have used $f_{\mathrm{SC}}\tau_L = f_{\mathrm{SC}}R_LC_L \gg 1$ and (6) and (7). This converges to $\overline{I_{\mathrm{OUT}}}R_L$ in steady state [see Fig. 6(b)], i.e., in the steady state, $\overline{I_{\mathrm{OUT}}}$ flows into the electrode to charge C_L, and then, exactly the same amount of charge leaks out through R_L as expected. This is equivalent to flowing $\overline{I_{\mathrm{OUT}}}$ through R_L. In fact, the overall voltage response of the R_LC_L load to the switched-capacitor current injector captured by (8), ignoring the ripples [ΔV_{OUT} of (6)], is identical to the voltage response of the R_LC_L load to an ideal step current with a magnitude $\overline{I_{\mathrm{OUT}}}$ [see Fig. 6(b)]. This justifies our current injector as a constant current injector. The foregoing discussion has assumed $\overline{I_{\mathrm{OUT}}}R_L < V_{\mathrm{DD}} - V_{\mathrm{OV}} - V_{\mathrm{SG}}$ (V_{OV}: overdrive voltage of the current mirror transistor); if $\overline{I_{\mathrm{OUT}}}R_L > V_{\mathrm{DD}} - V_{\mathrm{OV}} - V_{\mathrm{SG}}$, V_{OUT} will start to roll off and be clipped at V_{DD} [see Fig. 6(b)].

In the pCC mode, the current injector is connected to the electrode (so $V_e = V_{\mathrm{OUT}}$ and $I_e = I_{\mathrm{OUT}}$) and runs in parallel with the voltage amplifier [see Fig. 4(a)], where $\Delta V_{\mathrm{OUT}} = 0.1 \sim 50$ mV for $C_L = 1 \sim 100$ pF. This ripple voltage could interfere with the recording of $\Delta V_e = 1 \sim 30$ mV. We minimize this interference using clock synchronization (see Section IV-D).

C. Implementation

The actual switched-capacitor-based current injector that we implement is shown in Fig. 7(a). It can inject both positive and negative currents. The polarity is controlled by turning on either current source $I_{0,p}$ or $I_{0,n}$ to reduce the circuit to either Fig. 7(b) for positive injection, $\overline{I_{\mathrm{OUT}}} \approx f_{\mathrm{SC}}C_{\mathrm{SC}}V_{\mathrm{SG,PMOS}} > 0$, or Fig. 7(c) for negative injection, $\overline{I_{\mathrm{OUT}}} \approx -f_{\mathrm{SC}}C_{\mathrm{SC}}V_{\mathrm{GS,NMOS}} < 0$. For pCC recording, we use the NMOS configuration of Fig. 7(c) to set $I_e \sim -1$ nA, as negative current enables intracellular access [see Fig. 4(a)]. Here, we do not balance the negative injection with a positive injection for a given clock frequency in order to minimize the amount of circuitry and corresponding area: it is only used as a negative current injector for the intracellular experiments.

The bottom of Fig. 7(d) (solid red box) shows the transistor-level schematic of Fig. 7(a). The core switched-capacitor circuit uses two transmission gates and can add 10 or 100 fF to the parasitic capacitance $C_{\mathrm{SC},p} \sim 30$ fF of the V_{SC} node for C_{SC}. We remove the body effect of transistors M_n and M_p to minimize the $|V_{\mathrm{SG}}|$ dependence on V_{OUT} by tying the source and body nodes in both the PMOS and NMOS transistors (the 0.18-μm technology that we use is a triple-well process). A control signal $\mathrm{EN_{POS}}$ in the bias network enables either the $I_{0,p}$ or $I_{0,n}$ current sources of Fig. 7(a) for positive or negative injection. The clock can be selected from three clock inputs, CLK[1:3], and this enables flexible control of f_{SC} across the 4096 pixels.

D. Clock-Sampling Synchronization

As the current injector in the pCC configuration utilizes switched capacitances, f_{SC} is synchronized to the pixel multiplexer to minimize aliasing of switching induced noise, ΔV_{OUT} of (6), in the recorded amplifier output signal, V_{amp}. The aliased ΔV_{OUT} amplitude dominates the noise of the

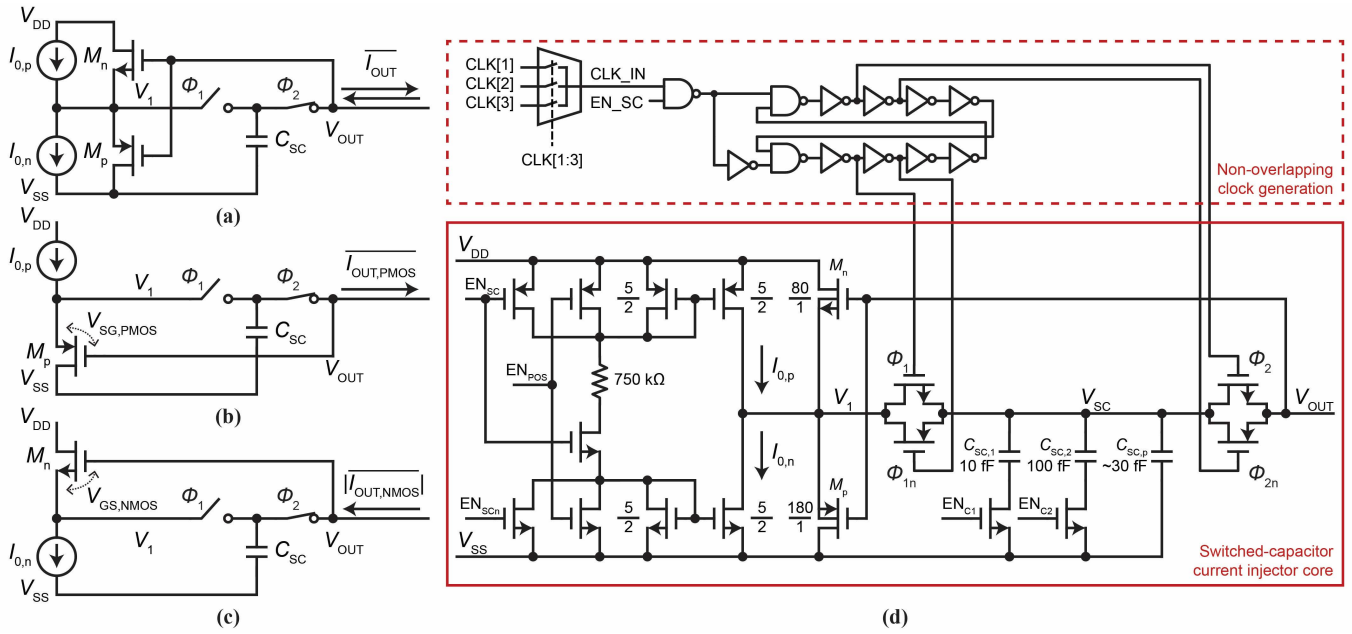


Fig. 7. (a) Current injector that we implement. (b) With $I_{0,p}$ ON and $I_{0,n}$ OFF, (a) is reduced to what is shown here, capable of positive current injection. (c) With $I_{0,n}$ ON and $I_{0,p}$ OFF, (a) is reduced to what is shown here, capable of negative current injection. (d) Transistor-level schematic of the current injector, including the non-overlapping clock generation circuit. Control signals CLK[1:3], $\mathrm{EN_{SC}}$, $\mathrm{EN_{POS}}$, $\mathrm{EN_{C1}}$, and $\mathrm{EN_{C2}}$ are controlled by the pixel's transparent latch memory.

pCC configuration and is larger than any parasitic charge injection or clock feedthrough as it is directly related to the discharging of the switched capacitor into the current injector's output node/input of the amplifier. To start, V_{amp} is sampled by a 128:1 output multiplexer [see Fig. 3(a) and (c)] operated at a frequency of $f_s \sim 1.2$ MHz resulting in a pixel sample frequency $f_{s,\mathrm{pixel}} = f_s/128 \sim 9.4$ kHz. To synchronize f_{SC} to $f_{s,\mathrm{pixel}}$ across all 128 pixels in the multiplexer, f_{SC} should be an integer multiple of $f_{s,\mathrm{pixel}}$ ($f_{\mathrm{SC}} = nf_{s,\mathrm{pixel}}$, $n = 1, 2, \ldots$), while f_s should be an integer multiple of f_{SC} ($f_s = mf_{\mathrm{SC}} = 128 f_{s,\mathrm{pixel}}$, $m = 1, 2, \ldots$). Taken together ($n \cdot m = 128$), f_{SC} must be a power of 2 multiple of $f_{s,\mathrm{pixel}}$ to eliminate aliasing ($f_{\mathrm{sc}} = 2^N f_{s,\mathrm{pixel}}$, $N = 0, 1, 2, \ldots$).

However, this constraint limits the resolution of injected current as $\overline{I_{\mathrm{OUT}}} \propto f_{\mathrm{SC}}$. To elaborate, the minimum $|\overline{I_{\mathrm{OUT}}}|$ at $f_{s,\mathrm{pixel}} \sim 9.4$ kHz would result in available $|\overline{I_{\mathrm{OUT}}}|$ of only 150 pA, 300 pA, 600 pA, 1.2 nA, 2.4 nA, and so on. To obtain a higher resolution in the injected current, a nonsymmetric clocking scheme is used for the generation of f_{SC} (see Fig. 8). Effective single integer multiples are established by spacing n pulses as evenly as possible with $1/f_s$ resolution throughout the total multiplexer period of $1/f_{s,\mathrm{pixel}} = 128/f_s$ [see Fig. 8(a)]. The resultant digital bitstream is then repeated at $128/f_s$ (equivalent to $1/f_{s,\mathrm{pixel}}$, $\sim$100 μs) to form a continuous output. The current resolution used for experiments is then $n \cdot 150$ pA, $n = 1, 2, \ldots, 64$. The non-symmetrical switching can increase ΔV_{OUT} by up to 50% at $n = 63$ [see Fig. 8(b)], yet the synchronization minimizes this increase from affecting the signal measurement. A dedicated microprocessor is used to generate the nonsymmetric clocks (CLK[1:3] in Fig. 7). During experiments (see Section VI-A), we observe low-frequency ΔV_{OUT} noise most likely due to clock drift between the microprocessor and acquisition electronics.

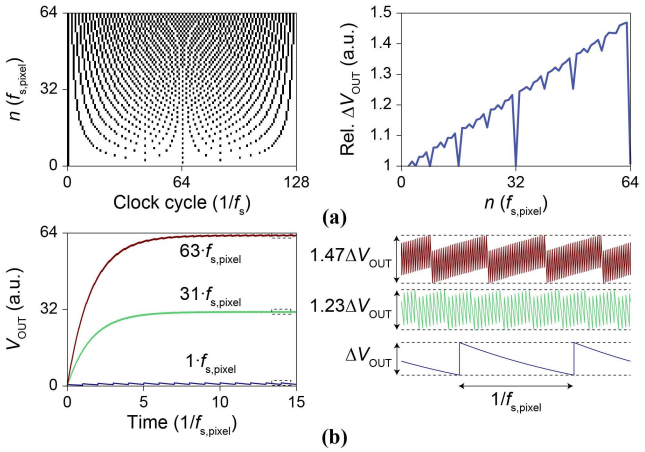


Fig. 8. (a) Left: pCC clocking scheme to synchronize the switched-capacitor current injector's f_{sc} to the multiplexer sampling at f_s. Black indicates f_{sc} high; white indicates f_{ss} low. The clock sequence is repeated after $128/f_s$. Right: ΔV_{OUT} is increased due to the scheme. (b) Simulated V_{OUT} traces for positive current injection for three different magnitudes and their steady state V_{OUT}(t) ripple voltage.

The same synchronization scheme is used for the pVC configuration, whose transimpedance amplifier also uses a switched capacitance. In this case, we commonly set $f_{\mathrm{TIA}} = 4 f_{s,\mathrm{pixel}} = 37.6$ kHz to minimize switching noise.

V. Electrical Characterization

A. Experimental Setup

The IC is packaged and placed on a printed circuit board (PCB) (see Fig. 9). The IC and PCB are programed and read through three National Instruments PXIe-6358 data acquisition (DAQ) cards and interfaced to a computer through

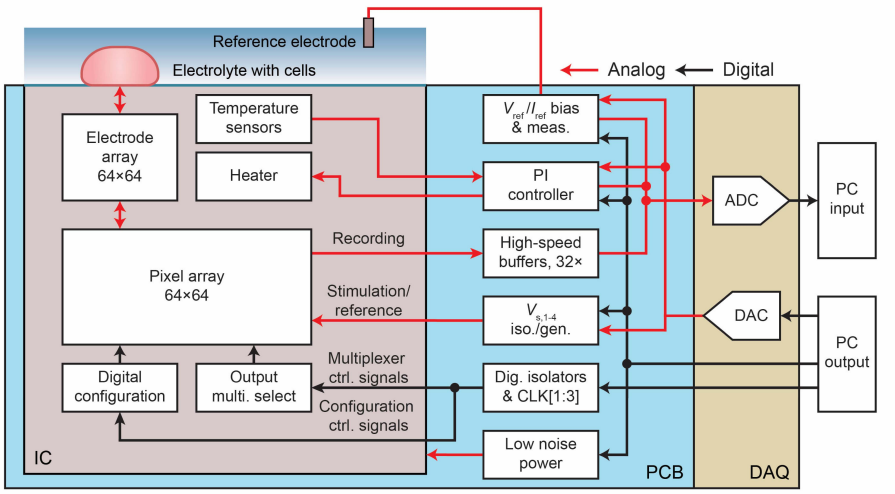


Fig. 9. System architecture of the IC and external electronics showing analog and digital signal flow.

LabVIEW software. For digital programming, each pixel is addressed in a shift register (4096 bits) with real-time adjustment/latching of the bit lines (B[1:25] in Fig. 3). For recording, the 4096 pixel amplifier outputs are divided into 32 subgroups. Each subgroup contains 128 outputs from two rows of the array, feeding its own 128:1 analog output multiplexer on chip. Each of the 32× distributed in-pixel multiplexers, as shown in Fig. 3(c), right, consumes 0.45 mW of total power; 32 NMOS source followers, each consuming 6.86 mW, are then used to buffer the 32× 128:1 multiplexer outputs from the IC to 32× 16 bit ADCs of the DAQ cards. Adjacent pixel-to-pixel crosstalk within the multiplexer was measured at −43 dB. The overall data rate of recording is 77 MB/s.

The IC's V_{SS} is set to earth ground and $V_{DD} = 3.6$ V; this is set higher than the 3.3-V transistors that we use, in order to increase both output and stimulation voltage ranges. The $V_{s,1}$–$V_{s,4}$ nodes are connected to DAQ analog outputs that are low-pass filtered ($f_{-3\,dB} \sim 1$ Hz) to provide bias voltages or buffered with a bandwidth of ∼100 kHz to provide voltage signals for various pixel circuit characterizations. The extracellular solution is biased using a Pt or Ag/AgCl reference electrode at V_{ref}, which is adjustable from 0 to 3.6 V. To regulate the temperature for cell health, the two temperature sensor signals from the IC are fed to an analog PI controller on the PCB, which then sets the voltage of a regulator on the PCB to drive the integrated heater. The designed accuracy for the temperature regulation is <1 °C and is calibrated using a thermocouple placed on the surface of the device in solution. In addition to the IC's total power dissipation of 1.25 W when the array is fully enabled, the heater typically dissipates 0.55 ∼ 0.85 W to maintain 35 °C (see Table I). This extra power dissipation is needed to overcome heat loss of the solution on top of the device to the ambient environment and contrasts with MEAs designed for interfacing to thermally insulating tissues or environments. Like the integrated pixel array, the PCB is designed to be highly configurable to ensure ample experimental flexibility and is adjusted using analog switches digitally controlled through a serial interface.

TABLE I
POWER CONSUMPTION OF THE CMOS DEVICE

Circuit	Power/Circuit
Operational amplifier (x4096)	225 µW
Current injector (x4096)	24 µW
Output multiplexer (x32)	7.3 mW
Fully enabled array power consumption	**1.25 W**
Maximum heater power	1.3 W
Typical heater power to maintain 35ºC	0.55 – 0.85 W

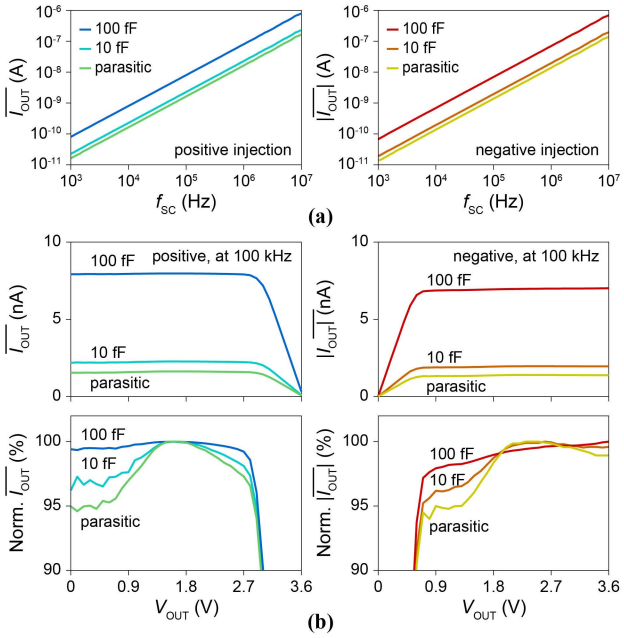


Fig. 10. (a) Positive and negative $\overline{I_{OUT}}$ versus f_{SC} for $V_{OUT} = 1.8$ V. (b) Positive and negative $\overline{I_{OUT}}$ versus V_{OUT} for $f_{SC} = 100$ kHz.

B. Measurement of Pixel Current Injector

We first characterize the pixel current injector by connecting V_{OUT} to the PCB via $V_{s,3}$, bypassing the pixel electrode and the solution. Fig. 10(a) shows the measured positive and

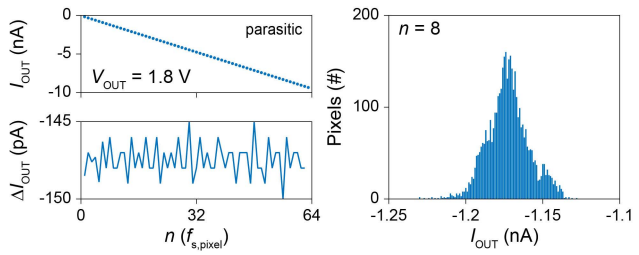


Fig. 11. Left: I_{OUT} versus n of the pCC clock synchronization scheme. Right: distribution of I_{OUT} at $n = 8$ for all 4096 pixels, bin size of 1 pA.

negative $\overline{I_{OUT}}$ versus f_{SC} (1 kHz∼10 MHz) for $V_{OUT} = V_{s,3} = 1.8$ V ($V_{DD} = 3.6$ V and $V_{SS} = 0$ V). They confirm the linear response of $|\overline{I_{OUT}}|$ to f_{SC} over the four decades of frequency, from which we extract $V_{SG,PMOS} = 0.63$ V, $V_{GS,NMOS} = 0.56$ V, and $C_{SC,p} = 26$ fF. The minimum $|\overline{I_{OUT}}|$ is ∼15 pA at $f_{SC} = 1$ kHz, and the maximum $|\overline{I_{OUT}}|$ is ∼0.7 μA at $f_{SC} = 10$ MHz.

To demonstrate the weak dependence of $\overline{I_{OUT}}$ on V_{OUT}, $V_{OUT} = V_{s,3}$ is swept from 0 to 3.6 V while fixing f_{SC} at 100 kHz. Both currents show flat responses [see Fig. 10(b)], with the positive $\overline{I_{OUT}}$ rolling off around V_{DD}-$V_{SG,PMOS}$ ∼ 3.0 V and the negative $\overline{I_{OUT}}$ rolling off around $V_{SS} + V_{GS,PMOS}$ ∼ 0.6 V. The measured variations of $|\overline{I_{OUT}}|$ in the flat regions are only within ∼5% for $C_{SC} = C_{SC,p}$. Its deviation from theoretical 0.3% is due mainly to the voltage dependence of $C_{SC,p}$ (for $C_{SC} = 100$ fF + $C_{SC,p}$ where the $C_{SC,p}$ effect is weaker, the current variation is reduced to <2%). In addition, this variation of $\Delta\overline{I_{OUT}}/\overline{I_{OUT}}$ ∼5% for the V_{OUT} sweep remains the same regardless of $f_{SC} \propto \overline{I_{OUT}}$ because Z_{OUT} is approximately inversely proportional to $\overline{I_{OUT}}$ [see (5)]. The discrete negative injection levels for the clock-sampling synchronization scheme (see Section IV-D) were then measured using $C_{SC} = C_{SC,p}$, i.e., the configuration used for the pCC intracellular measurements. For the pixel shown in Fig. 11, left, $\overline{I_{OUT}}$ is at distinct multiples of −147 pA, corresponding to $nf_{s,pixel}$. At $n = 8$, $\overline{I_{OUT}}$ shows <5% variation around ∼ −1.2 nA across the array.

To measure the output ripple voltage ΔV_{OUT} [see (6)] and to highlight the ability for small amplitude current injection, the current injector was tested in a solution using a small, 2-μm-diameter Pt electrode (with no PtB deposition) post-fabricated on the pixel pad. This post-fabrication involves photolithography to define the hole, dry etching of the foundry passivation to expose the Al pad, deposition of 20-nm Ti and 200-nm Pt, and liftoff [31]. The pixel op-amp was configured as a buffer to measure the voltage ripple during the current injection. We increase f_{SC} from 0 Hz to 1 kHz and then decrease it back to 0 Hz, all in 200-Hz increments (see Fig. 12, bottom). This results in ∼5-pA step current increases/decreases for positive/negative injections (see Fig. 12, top). The ripple voltage can be clearly seen (see Fig. 12, middle, at $f_{SC} = 600$ Hz), with ∼20-mV step size for both positive and negative injections. This ripple voltage for the 2-μm-diameter Pt electrode with $C_L = 1.7$ pF being much larger (est. 50×) than the ripple voltage for the PtB electrode that has a much larger C_L due to its rough surface texture that

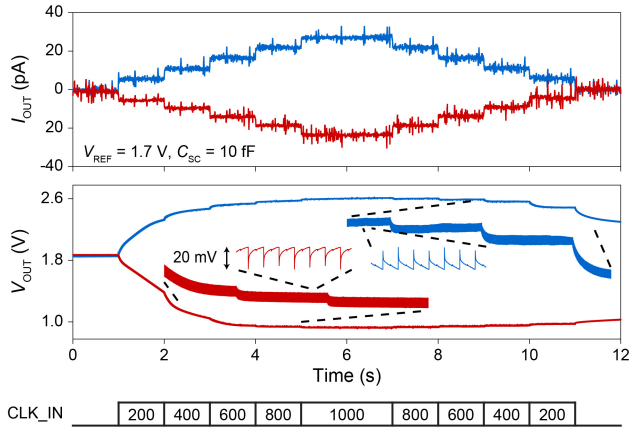


Fig. 12. Small amplitude current injection measurement in solution with a post-fabricated Pt electrode. An Ag/AgCl reference was used at $V_{REF} = 1.7$ V to set V_{OUT} to ∼1.8 V. Insets: ripple voltage of V_{OUT} for $f_{SC} = 600$ Hz.

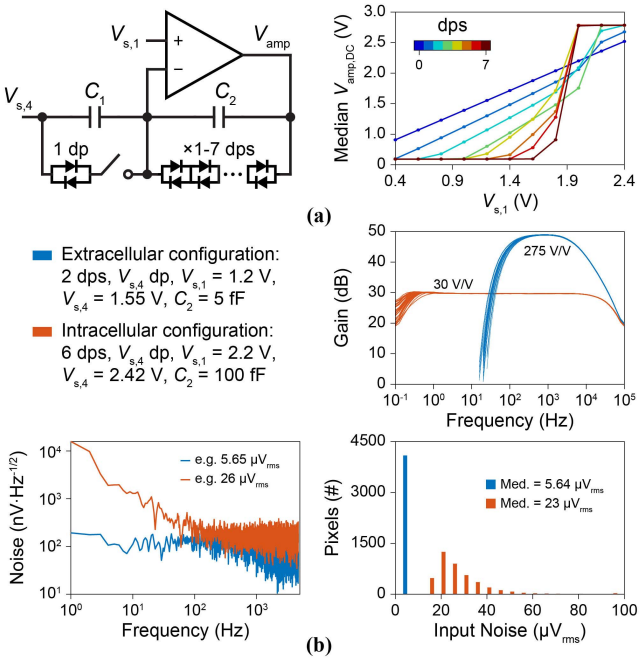


Fig. 13. pCC amplifier characterization. (a) Array's median $V_{amp,dc}$ versus $V_{s,1}$ for each of the one-to-seven feedback dp options (without the $V_{s,4}$ dp). (b) Measurements of the extracellular and intracellular configurations: gain versus frequency for 32 pixels, input-referred noise for a single example pixel, and input-referred noise integrated from 1 Hz to 4.7 kHz across the array.

increases its surface area. These time-dependent behaviors of $|\overline{I_{OUT}}|$ and V_{OUT} are consistent with the theoretical considerations of Section IV-B (see Fig. 6).

C. Measurement of pCC and pVC Amplifiers

The pCC amplifier configuration was first tested to investigate the optimal number of feedback dps for voltage amplification: the input ($V_{s,1}$) and output (V_{amp}) dc transfer curve was measured for each of the 0–7-dps options across the array [see Fig. 13(a)]. This test is important to ensure array-wide operation: leakage currents across the multiple feedback dps can induce offset voltages that can saturate the amplifier, reducing the number of available pixels. Sharp transitions of

the array wide median $V_{\text{amp,dc}}$ from the lower (0.2 V) to upper (2.8 V) output voltage rails for increasing the number of feedback dps show their sensitivity to the leakage currents (see Fig. 13(a), right). To overcome this sensitivity, not only do we choose the optimal number of feedback dps but we also use the dp connected to $V_{s,4}$ to set a current across the feedback dps to tune their offset and impedance.

For the extracellular recording of the membrane potential (this is done later in Section VI by setting $I_e = 0$ in the pCC configuration so as not to cause membrane permeabilization), we use two feedback dps in parallel to $C_2 = 5$ fF to set a passband gain of 275 V/V with a bandwidth $f_1 = 100$ Hz to $f_2 = 5$ kHz [see Fig. 13(b)]. The 100-Hz pole substantially filters out the $1/f$ noise, given that the open-loop amplifier has a $1/f$ noise corner of ~10 Hz. The measured input-referred noise is 5.6 μV_{rms} when integrated from 1 Hz to 4.7 kHz [see Fig. 13(b)].

The pCC intracellular recording mode (done later in Section VI with non-zero I_e) must deal with larger amplitude signals ($\Delta V_e > 1$ mV or $\Delta V_{\text{amp}} > 300$ mV). In this case, since the two feedback dps exhibit non-linear clipping, we instead use six feedback dps to lessen the voltage seen on each dp with large output voltages. In this configuration, the feedback current is especially essential to control $V_{\text{amp,dc}}$ across the array that would otherwise be saturated due to the sharp slope observed in Fig. 13(a) with 6 dps. With this measure, signals as large as $\Delta V_e > 20$ mV can be recorded without distortion. On the other hand, the large impedance of the 6 dps causes $f_1 < 1$ Hz; this lets in a larger amount of $1/f$ noise (as the open-loop amplifier has the $1/f$ corner at ~10 Hz), resulting in an increased integrated input-referred noise of ~23 μV_{rms} at $A_v = 30$ V/V [see Fig. 13(b)]. Digital filters can reduce this additional low-frequency noise depending upon the signal frequencies of interest (e.g., PSPs range from ~100 Hz to 1 kHz).

Fig. 14 shows the characterization of the pVC transimpedance amplifier. Input current I_{in} is applied using $V_{s,4}$ through $C_1 = 3.5$ pF (see Fig. 14(a), left) to measure the transimpedance gain $R_{\text{TIA}} \sim 700$ MΩ for $f_{\text{SC,pVC}} = 4f_{s,\text{pixel}} = 37.6$ kHz and for $V_{s,1} = 1.0$ ~2.4 V (see Fig. 14(a), right). The bandwidth of the transimpedance amplifier extends from dc to 2-kHz set by R_{TIA} and $C_2 = 100$ fF (see Fig. 14(b), left) with an input-referred noise as low as 1.1-pA_{rms} integrated from 1 Hz to 4.7 kHz (see Fig. 14(b), right). Gain and noise measurements across the array show a distinct spatial dependence due to multiplexer sampling and its relation to the clock phases [see Fig. 14(c)]: pixels that are sampled during Φ_1 exhibit larger noise and gain in comparison to Φ_2. These variations could be optimized in future designs by incorporating a dedicated switched feedback element synched to the multiplexer in the pixel circuit and using a traditional integrate and reset method for the lowest noise performance [35].

D. Characterization of Electrode and Routing Capacitance

For optimal pCC and pVC coupling [see (1)–(4)], we desire a small electrode impedance (Z_e) or a large electrode capacitance C_e. Concretely, $C_e \gg (C_{p,r} + C_1)$ is the condition

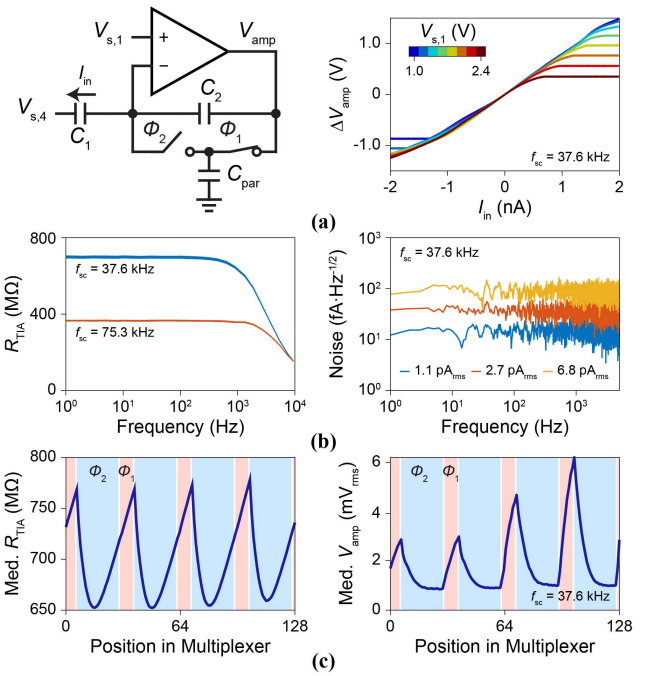


Fig. 14. (a) Left: pVC transimpedance amplifier measurement setup. Right: measured transimpedance with 2.5-ms I_{in} pulse inputs ($V_{s,1}$: 1.0 ~ 2.4 V). (b) Left: transimpedance gain, R_{TIA} versus frequency for 32 pixels for $f_{\text{SC,pVC}} = 37.6$ and 75.3 kHz. Right: input-referred current noise for 3 pixels. (c) Median R_{TIA} and V_{amp} voltage noise of 128 pixels sharing an output multiplexer.

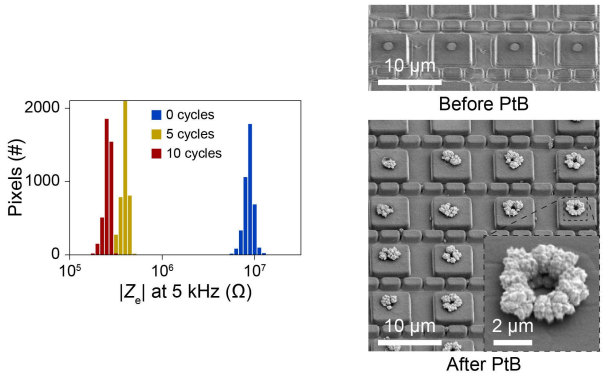


Fig. 15. Left: $|Z_e|$ at 5 kHz measured across the array during PtB deposition. Right: SEM images of planar hole electrodes before and after PtB deposition.

to obtain the final expression in (1), eliminating the attenuation due to the electrode; $|Z_e| \ll R_s$, R_{jm}, is the condition to obtain the final expressions of (3) and (4) with no attenuation due to the electrode. To minimize Z_e (i.e., to increase C_e), PtB is electrodeposited onto Pt electrodes post-fabricated on the Al pads, as the surface roughness of PtB increases the electrode surface area (e.g., Fig. 15, right) [31]. For the PtB deposition, $V_{s,1}$ is used to apply a voltage ramp to V_e from 0 to −1.2 V at 50 mV/s with respect to a Pt reference in a solution of 0.5-mM H_2PtCl_6 and 25-mM $NaNO_3$ [36]. Z_e is measured across the array periodically throughout the deposition by applying a 1–25-mV, 5-kHz sine wave sequentially to each pixel and measuring the resultant current through the

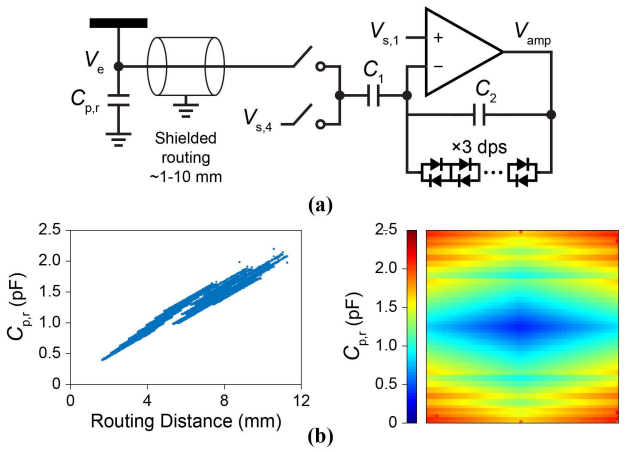


Fig. 16. (a) Configuration for measurement of $C_{p,r}$. (b) Left: dependence of $C_{p,r}$ on the electrode pixel routing distance. Right: heat map across the array.

reference electrode (see Fig. 15, left). Z_e is reduced by almost two orders, e.g., in Fig. 15, it is reduced to ∼300 kΩ ($C_e \sim 100$ pF).

This C_e satisfies $C_e \gg (C_{p,r} + C_1)$ for the final expression of (1) to hold, with $C_1 \sim 3.5$ pF and $C_{p,r} \sim 600$ fF–2 pF, depending on the routing length. We extract this $C_{p,r}$ by comparing the amplifier gain measured from $V_{s,1}$ to V_{amp} with C_1 connected to $V_{s,4}$ at the ground and the same gain but with C_1 connected to V_e (see Fig. 16). Also, $|Z_e| \ll R_s$, and R_{jm} for (3) and (4) is satisfied with R_s and R_{jm} in the MΩ range. The electrode-to-electrode coupling was also measured in a similar manner by applying a 1-V ac signal to all V_e's but the pixel measured: a total of 3.0 fF of electrode-to-electrode capacitance was measured, of which 2.3 fF was due to adjacent electrode pads, while 0.7 fF was from pixel circuit to electrode routing cross-coupling capacitance.

Beyond reducing Z_e, the surface roughness of the PtB also strongly interacts with the cell membrane to form a tight seal [31], increasing R_s. This not only further ensures $|Z_e| \ll R_s$, R_{jm} for (3) and (4) to be valid for the pVC operation but also reduces the attenuation of the pCC recording [see (1)] and enhances the pCC stimulation effectiveness [see (2)].

VI. Electrophysiological Measurements

We demonstrate pCC and pVC intracellular recording and stimulation with dissociated rat neurons, cultured on the IC for 10–14 days *in vitro*. We use PtB vertical nanoneedles for pVC and PtB vertical nanoneedles with pad edge electrodes for pCC [31]. Fig. 17 shows an example extracellular signals recorded using the high-gain, low-noise voltage amplifier configuration of our CMOS IC—-similar to other CMOS MEAs [1]–[14]—-as a reference for comparison to the intracellularly recorded signals that we will present now.

A. pCC Neuron Measurements

To demonstrate the pCC operation, we first determined the threshold I_e needed for intracellular access by changing I_e

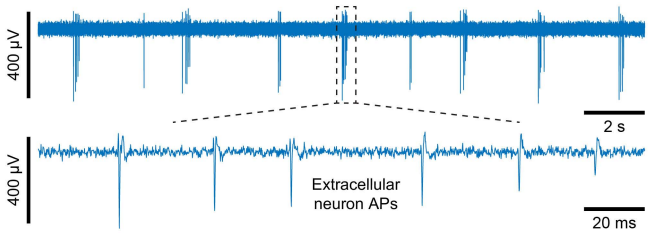


Fig. 17. Example of the extracellular recording of a dissociated rat neuron using a PtB planar hole electrode.

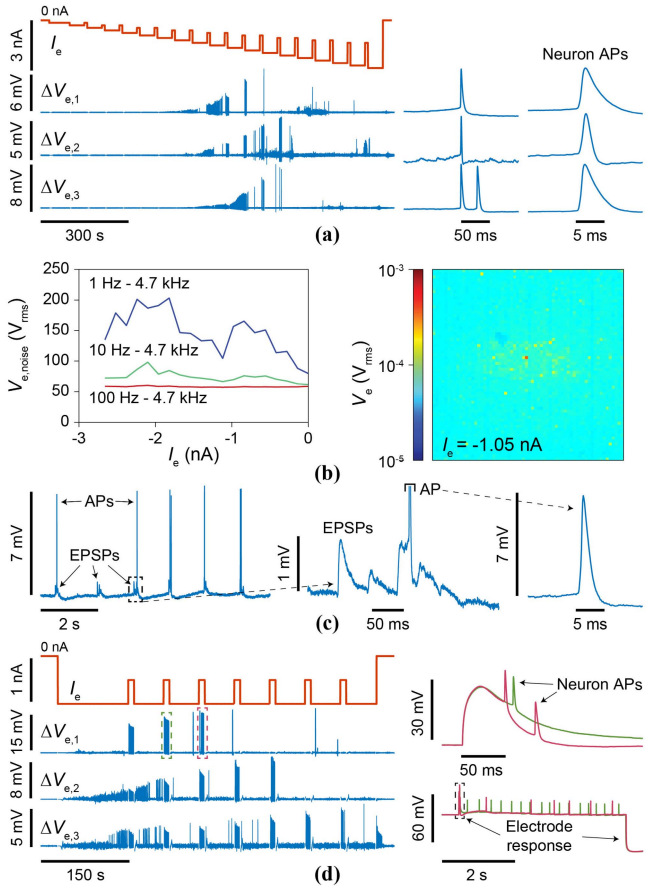


Fig. 18. (a) Ramped experiment to determine intracellular threshold I_e with dissociated rat neurons. (b) Integrated $V_{e,\text{noise}}$ for an individual pixel without an interfacing neuron (left) and V_e amplitude-integrated from 100 Hz to 4.7 kHz across the array below the threshold for the experiment of (a). (c) EPSP measurement. (d) Stimulation is achieved through the adjustment of I_e.

from 0 ∼ −3.0 nA with a step of −150 pA and measuring V_e with the rat neurons on top [see Fig. 18(a)]. The threshold I_e was determined when V_e substantially increased, and APs were clearly distinguished [see Fig. 18(a)]. The intracellular threshold so determined lied between −1.1 to −2.2 nA across the array.

To quantify the overall noise at the electrode beyond the input-referred noise of the pCC amplifier, we performed two types of experiments. First, we measured V_e for various bandwidths again by changing I_e from 0∼ −3.0 nA, but this time without a neuron above (Fig. 18(b), left shows the data for an

TABLE II

PERFORMANCE COMPARISON OF STATE-OF-THE-ART CMOS MICROELECTRODE AND NANOELECTRODE ARRAYS

		[3]	[4], [14]	[5]	[6]	[25] (Our prior work)	This work
Technology node		0.18 µm	0.18 µm	0.13 µm	0.13 µm	0.35 µm	0.18 µm
Electrode shape		Planar microelectrode with surface roughness	Planar microelectrode	Planar microelectrode	Planar microelectrode	Vertical nanoelectrode	Vertical nanoelectrode with surface roughness
Electrode pitch		13.5 µm	25.5 µm	58 µm	15 µm	126 µm	20 µm
No. electrodes		59,760	65,536	1,024	16,384	1,024	4,096
No. recording channels		2,048	65,536	4	1,024	1,024	4,096
Cell-electrode interface modality	Extracellular voltage recording	Yes	Yes	Yes	Yes	Yes	Yes
	Intracellular voltage recording with no concurrent stimulation	-	-	-	Yes (cardiomyocyte)	Yes (cardiomyocyte)	Yes (cardiomyocyte)
	Intracellular voltage recording with current injection (current clamp)	-	-	-	-	-	Yes (neuron)
	Intracellular current recording with voltage application (voltage clamp)	-	-	-	-	-	Yes (neuron)
	Constant voltage stimulation (CVS)	Yes	Yes	-	Yes	Yes	Yes
	Constant current stimulation (CCS)	Yes	-	Yes	Yes	-	Yes
	Impedance monitoring	-	-	-	Yes	-	-
	Impedance spectroscopy	Yes	-	Yes	Yes	-	-
	Chemical	Yes	-	-	-	-	-
No. stimulation waveform generation units		16 (V or I)	External (V)	4 (I)	64 (V) + 64 (I)	External (V)	External (V) + 4,096 (I)
No. stimulation waveforms		6 (V or I)	1 (V)	4 (I)	64 (V) + 64 (I)	3 (V)	3 (V) + 3 (I)
No. sites for simultaneous CVS		N/A	65,536	-	4,096	1,024	4,096
No. sites for simultaneous CCS		6	-	4	64	-	4,096
CVS/CCS range		±1.5 V / ±300 µA	3.3 V / -	- / ± 32 µA	± 1.65 V / ± 382.5 nA	4 V / -	3 V / ± 300 µA
CVS/CCS resolution (LSB)		2.9 mV / 29 nA	N/A	250 nA	103 mV / 2 pA	-	- / 5 pA (140 pA for pCC)
Channel gain		30-7000	50-250	22-412	2-3000	150-375	30-275
Channel bandwidth (maximum)		1 Hz - 10 kHz	100 Hz - 10 kHz	0.1 Hz - 26 kHz	0.5 Hz - 10 kHz,	1 Hz - 5 kHz	<1 Hz to 30 kHz
Input-referred noise (rms)	Full band	5.4 µV		12.6 µV	12 µV	250 µV	23 µV
	AP band	2.4 µV	10 µV	7 µV	7.5 µV		5.6 µV
ADC		10b @ 20 kS/s	External	External	10b @ 20 kS/s	External	External
Temperature control		Yes (temp. sensor)	-	-	-	-	Yes (temp. sensor with heater and external PID controller
Total power		86 mW	153 mW	N/A	95 mW	12 mW	1.25 W (w/o heater)

example pixel). Second, we measured V_e with the I_e below the intracellular threshold so that no intracellular coupling occurs even if there is a neuron above (Fig. 18(b), right shows the data across the array). These experiments show that on top of the ~23-μV_{rms} input-referred noise of the pCC intracellular-mode amplifier (see Section V-C), there is an additional noise

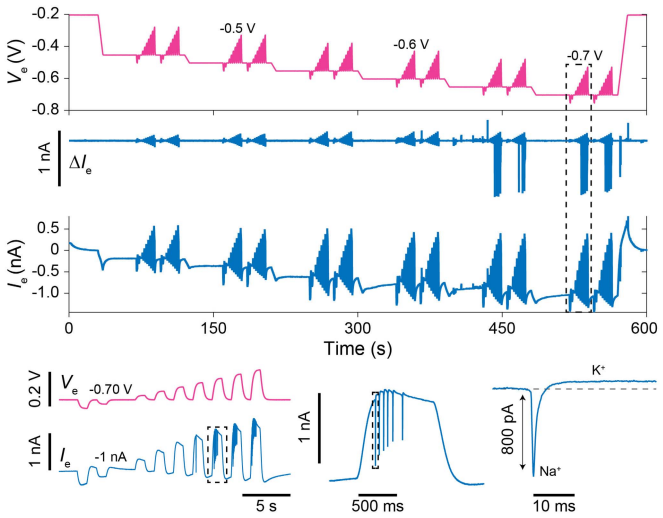


Fig. 19. Ramped V_e experiments in the pVC configuration to determine the threshold for intracellular access using a PtB nanoneedle electrode and dissociated rat neurons. V_e stimulations are applied to activate ion channels.

of $40 \sim 150$ μV_{rms} largely below 10 Hz in frequency. This extra noise originates from the electrode ($\sim$10 μV_{rms}), solution ($\sim$30 μV_{rms} [12]), and the current injector's ripple voltage ($0 \sim 110$ μV_{rms}, dependent upon $|I_e|$). If the clock of the switched-capacitor current injector and that of the output multiplexer were perfectly synchronized, the ripple voltage noise would disappear in its entirety (see Section IV-D), but, in reality, the two clocks slightly drift from each other at low frequencies below 10 Hz, which aliases the ripple voltage into the recording noise at the low frequencies. The non-uniformity of the noise across the array (see Fig. 18(b), right) is attributed to variations in f_1 arising from feedback diode leakage current variation. By comparing this overall noise to the AP amplitudes of $1 \sim 30$ mV measured at the electrode in the pCC intracellular mode (e.g., Fig. 18(a), right), we obtain a signal-to-noise ratio $>$20, on par with the patch clamp. The signal-to-noise ratio for PSPs is also $>$1, so subthreshold (synaptic) signal measurement is also possible. An example of such subthreshold sensitivity is shown in Fig. 18(c), where excitatory PSPs (EPSPs) are clearly measured with ΔV_e amplitudes of $\sim$200 μV–$\sim$1 mV at the electrode.

A stimulation experiment with intracellular coupling at $I_e \sim -1.1$ nA with periodic +550-pA injections [see Fig. 18(d)], during which increased neuron AP firings are observed, demonstrates the ability to intracellularly record ΔV_e and adjust I_e simultaneously to stimulate the neuron through the same electrode.

The scalability of the device for network-wide intracellular recording was demonstrated with an intracellular measurement of more than 1700 neurons in parallel for a $>$40% intracellular coupling rate [31]. The subthreshold sensitivity enabled cross-pixel AP to PSP correlation that allowed mapping of 304 synapses between 396 neurons, which demonstrates the capability of the IC for synaptic connectivity mapping applications [31].

B. pVC Neuron Measurements

To demonstrate the pVC operation, we gradually increased the magnitude of V_e to determine the threshold for intracellular access (see Fig. 19). Since no spontaneous activity is observed for pVC due to its low input impedance, voltage stimulations were applied to activate the neuron's ion channels: at $V_e = -0.65$ to -0.7 V, distinct Na^+ spikes and K^+ repolarization currents are observed during stimulation, clearly distinguished in the high-pass (100-Hz) filtered version of the measured electrode current ΔI_e. The pVC mode clearly enables the ability to measure I_e and adjust V_e simultaneously, allowing for the concurrent intracellular recording of ion channel currents and stimulation of membrane potentials.

Such intracellular ion-channel measurement of mammalian neurons can be useful for high-throughput drug screening applications, where current high-throughput intracellular tools, i.e., the planar patch clamp, are limited to non-neuronal, artificial cell lines. As a first demonstration toward this end, we measured the effects of ion-channel drugs affecting both the Na^+ and K^+ currents of the dissociated rat neurons [31].

VII. Conclusion

We have presented the CMOS IC that contains 4096 pCC/pVC pixel circuits, with each connected to a PtB electrode. The electrodes form a dense, 20-μm pitch 64×64 array. Overall, the IC enables large-scale intracellular recording of neurons with the ability of simultaneous excitations. It is the flexibility of the pixel circuit, containing a new switched-capacitor-based current injector and a highly configurable op-amp, that enables both the pCC and pVC modes within each pixel circuit. The lateral separation of the pixel circuit from the electrode decouples the electrode pitch from the larger pixel circuit area for the low-noise design with the high configurability. The device has been fabricated in 0.18-μm CMOS technology, electrically characterized, and verified biologically with *in vitro* rat neurons. We summarize and compare the performance of this CMOS nanoelectrode array to start-of-the-art CMOS MEAs as well as our prior CMOS nanoelectrode array in Table II [3]–[6], [14], [25].

References

[1] B. Eversmann *et al.*, "A 128 × 128 CMOS biosensor array for extracellular recording of neural activity," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2306–2317, Dec. 2003.

[2] F. Heer, S. Hafizovic, W. Franks, A. Blau, C. Ziegler, and A. Hierlemann, "CMOS microelectrode array for bidirectional interaction with neuronal networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1620–1629, Jul. 2006.

[3] J. Dragas *et al.*, "*In vitro* multi-functional microelectrode array featuring 59 760 electrodes, 2048 electrophysiology channels, stimulation, impedance measurement, and neurotransmitter detection channels," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1576–1590, Jun. 2017.

[4] D. Tsai, R. Yuste, and K. L. Shepard, "Statistically reconstructed multiplexing for very dense, high-channel-count acquisition systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 1, pp. 13–23, Feb. 2018.

[5] J. S. Park *et al.*, "1024-pixel CMOS multimodality joint cellular sensor/stimulator array for real-time holistic cellular characterization and cell-based drug screening," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 1, pp. 80–94, Feb. 2018.

[6] C. M. Lopez *et al.*, "A multimodal CMOS MEA for high-throughput intracellular action potential measurements and impedance spectroscopy in drug-screening applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3076–3086, Nov. 2018.

[7] L. Berdondini *et al.*, "Active pixel sensor array for high spatio-temporal resolution electrophysiological recordings from single cell to large scale neuronal networks," *Lab Chip*, vol. 9, no. 18, p. 2644, 2009.

[8] U. Frey *et al.*, "Switch-matrix-based high-density microelectrode array in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 467–482, Feb. 2010.

[9] P. Livi, F. Heer, U. Frey, D. J. Bakkum, and A. Hierlemann, "Compact voltage and current stimulation buffer for high-density microelectrode arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 372–378, Dec. 2010.

[10] R. Huys *et al.*, "Single-cell recording and stimulation with a 16k micro-nail electrode array integrated on a 0.18 μm CMOS chip," *Lab Chip*, vol. 12, no. 7, p. 1274, 2012.

[11] M. Ballini *et al.*, "A 1024-channel CMOS microelectrode array with 26,400 electrodes for recording and stimulation of electrogenic cells *in vitro*," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2705–2719, Nov. 2014.

[12] M. E. J. Obien, K. Deligkaris, T. Bullmann, D. J. Bakkum, and U. Frey, "Revealing neuronal function through microelectrode array recordings," *Frontiers Neurosci.*, vol. 8, p. 423, Jan. 2015.

[13] J. Müller *et al.*, "High-resolution CMOS MEA platform to study neurons at subcellular, cellular, and network levels," *Lab Chip*, vol. 15, no. 13, pp. 2767–2780, 2015.

[14] D. Tsai, D. Sawyer, A. Bradd, R. Yuste, and K. L. Shepard, "A very large-scale microelectrode array for cellular-resolution electrophysiology," *Nature Commun.*, vol. 8, no. 1, pp. 1–11, Dec. 2017.

[15] D. A. Wagenaar, J. Pine, and S. M. Potter, "Effective parameters for stimulation of dissociated cultures using multi-electrode arrays," *J. Neurosci. Methods*, vol. 138, nos. 1–2, pp. 27–37, Sep. 2004.

[16] O. P. Hamill, A. Marty, E. Neher, B. Sakmann, and F. J. Sigworth, "Improved patch-clamp techniques for high-resolution current recording from cells and cell-free membrane patches," *Pflügers Archiv Eur. J. Physiol.*, vol. 391, no. 2, pp. 85–100, Aug. 1981.

[17] A. Verkhratsky, O. A. Krishtal, and O. H. Petersen, "From Galvani to patch clamp: The development of electrophysiology," *Pflügers Archiv-Eur. J. Physiol.*, vol. 453, no. 3, pp. 233–247, Nov. 2006.

[18] R. Perin, T. K. Berger, and H. Markram, "A synaptic organizing principle for cortical neuronal groups," *Proc. Nat. Acad. Sci. USA*, vol. 108, no. 13, pp. 5419–5424, Mar. 2011.

[19] X. Duan *et al.*, "Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor," *Nature Nanotechnol.*, vol. 7, no. 3, pp. 174–179, Mar. 2012.

[20] C. Xie, Z. Lin, L. Hanson, Y. Cui, and B. Cui, "Intracellular recording of action potentials by nanopillar electroporation," *Nature Nanotechnol.*, vol. 7, no. 3, pp. 185–190, Mar. 2012.

[21] A. Hai and M. E. Spira, "On-chip electroporation, membrane repair dynamics and transient in-cell recordings by arrays of gold mushroom-shaped microelectrodes," *Lab Chip*, vol. 12, no. 16, pp. 2865–2873, 2012.

[22] N. Shmoel, N. Rabieh, S. M. Ojovan, H. Erez, E. Maydan, and M. E. Spira, "Multisite electrophysiological recordings by self-assembled loose-patch-like junctions between cultured hippocampal neurons and mushroom-shaped microelectrodes," *Sci. Rep.*, vol. 6, no. 1, p. 1, Jun. 2016.

[23] J. T. Robinson, M. Jorgolli, A. K. Shalek, M.-H. Yoon, R. S. Gertner, and H. Park, "Vertical nanowire electrode arrays as a scalable platform for intracellular interfacing to neuronal circuits," *Nature Nanotechnol.*, vol. 7, no. 3, pp. 180–184, Mar. 2012.

[24] Z. C. Lin, C. Xie, Y. Osakada, Y. Cui, and B. Cui, "Iridium oxide nanotube electrodes for sensitive and prolonged intracellular measurement of action potentials," *Nature Commun.*, vol. 5, no. 1, May 2014.

[25] J. Abbott *et al.*, "CMOS nanoelectrode array for all-electrical intracellular electrophysiological imaging," *Nature Nanotechnol.*, vol. 12, no. 5, pp. 460–466, May 2017.

[26] M. Dipalo *et al.*, "Intracellular and extracellular recording of spontaneous action potentials in mammalian neurons and cardiac cells with 3D plasmonic nanoelectrodes," *Nano Lett.*, vol. 17, no. 6, pp. 3932–3939, Jun. 2017.

[27] R. Liu *et al.*, "High density individually addressable nanowire arrays record intracellular activity from primary rodent and human stem cell derived neurons," *Nano Lett.*, vol. 17, no. 5, pp. 2757–2764, May 2017.

[28] D. Braeken *et al.*, "Open-cell recording of action potentials using active electrode arrays," *Lab Chip*, vol. 12, no. 21, p. 4397, 2012.

[29] M. Dipalo *et al.*, "Plasmonic meta-electrodes allow intracellular recordings at network level on high-density CMOS-multi-electrode arrays," *Nature Nanotechnol.*, vol. 13, no. 10, pp. 965–971, Oct. 2018.

[30] J. Abbott, T. Ye, D. Ham, and H. Park, "Optimizing nanoelectrode arrays for scalable intracellular electrophysiology," *Accounts Chem. Res.*, vol. 51, no. 3, pp. 600–608, Mar. 2018.

[31] J. Abbott *et al.*, "A nanoelectrode array for obtaining intracellular recordings from thousands of connected neurons," *Nature Biomed. Eng.*, vol. 4, no. 2, pp. 232–241, Feb. 2020.

[32] D. De Dorigo *et al.*, "Fully immersible subcortical neural probes with modular architecture and a delta-sigma ADC integrated under each electrode for parallel readout of 144 recording sites," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3111–3125, Nov. 2018.

[33] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

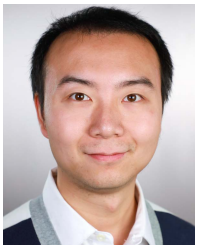
[34] M. E. Spira and A. Hai, "Multi-electrode array technologies for neuroscience and cardiology," *Nature Nanotechnol.*, vol. 8, no. 2, pp. 83–94, Feb. 2013.

[35] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise limits of CMOS current interfaces for biosensors: A review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 278–292, Apr. 2014.

[36] L.-L. Li, C.-W. Chang, H.-H. Wu, J.-W. Shiu, P.-T. Wu, and E. W.-G. Diau, "Morphological control of platinum nanostructures for highly efficient dye-sensitized solar cells," *J. Mater. Chem.*, vol. 22, no. 13, p. 6267, 2012.

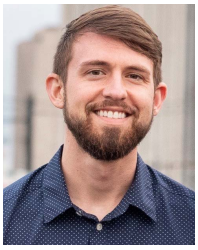
Jeffrey Abbott received the B.S./M.S. degree in electrical engineering from the Rochester Institute of Technology, Rochester, NY, USA, in 2011, and the Ph.D. degree in engineering sciences from the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA, in 2017.

He is currently a Post-Doctoral Fellow with the labs of Prof. Hongkun Park and Prof. Donhee Ham at Harvard University. His current research interests include analog integrated circuits, applications of nanotechnology to neuroscience, and high-throughput CMOS biosensors.



Tianyang Ye received the B.S. degree in microelectronics from Peking University, Beijing, China, in 2013, and the Ph.D. degree from Harvard University, Cambridge, MA, USA, in 2020.

He is currently a Post-Doctoral Fellow in Prof. Hongkun Park's lab at Harvard University. His current research interests include nanoscience, developing novel nanobiointerfaces, and building high-throughput electrophysiology platforms for *ex vivo* systems.



Keith Krenek received the B.S. and M.S. degrees in electrical engineering from Texas A&M University, College Station, TX, USA, in 2014 and 2015, respectively, and the Ph.D. degree in applied physics from Harvard University, Cambridge, MA, USA, in 2019.

His research interests include biosensors and microfluidics, photonic integrated circuits, rapid prototyping applied in new fields, guidance and navigation systems, and ionizing radiation physics.

Ling Qin received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2000, and the Ph.D. degree in engineering sciences from the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA, in 2017.

He is currently a SerDes Design Engineer with Apple Inc., Newton, MA, USA. His current research interests include analog and mixed-signal integrated circuits, high-speed links, sensors, and silicon–cell interface.

Youbin Kim received the B.A. degree in physics from Harvard University, Cambridge, MA, USA, in 2018. He is currently pursuing the Ph.D. degree in electrical engineering with the University of California at Berkeley (UC Berkeley), Berkeley, CA, USA.

His research interests include digital integrated circuits, computer architecture, and the design of hardware accelerators for high-dimensional computing and machine learning algorithms.

Wenxuan Wu (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering with a minor in chemistry from the University of Washington, Seattle, WA, USA, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering with the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA.

His current research interests include integrated circuit design for neurosciences, mixed-signal circuit design, and bioelectronic interface design.

Rona S. Gertner received the B.A. degree in biochemistry from Brandeis University, Waltham, MA, USA, in 1996, and the M.Sc. and Ph.D. degrees in biology from the Weizmann Institute of Science, Rehovot, Israel, in 2001 and 2007, respectively.

Since 2009, she has been a Research Assistant with the laboratory of Prof. Hongkun Park at the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA, USA.

Hongkun Park received the B.S. degree in chemistry from Seoul National University, Seoul, South Korea, in 1990, and the Ph.D. degree in chemistry from Stanford University, Stanford, CA, USA, in 1996.

He is currently a Mark Hyman Jr. Professor of chemistry and a Professor of physics with Harvard University, Cambridge, MA, USA. His current research interests include solid-state quantum optoelectronics, quantum sensing and control, and nanobiointerfacing.

Donhee Ham (Senior Member, IEEE) received the B.S. degree (*summa cum laude*) in physics from Seoul National University, Seoul, South Korea, in 1996. Following 1.5 years of military service in the South Korea Army, he went to the California Institute of Technology, Pasadena, CA, USA, for graduate training in physics under Barry Barish, and later received the Ph.D. degree in electrical engineering in 2002, winning the Charles Wilts Prize.

He is currently a Gordon McKay Professor of applied physics and electrical engineering with Harvard University, Cambridge, MA, USA, and a fellow of Samsung Electronics, Suwon, South Korea. His current research focus relevant to this article is CMOS-biointerfaces for neuroscience, machine intelligence, and biological data archiving.

Dr. Ham's other work experiences include the Caltech-MIT Laser Interferometer Gravitational Wave Observatory (LIGO), the IBM T. J. Watson Research, the technical program committees in the IEEE International Solid-State Circuits Conference and the IEEE Asian Solid-State Circuits Conference, an Advisory Board of the IEEE International Symposium on Circuits and Systems, a guest editorship for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and an Associate Editor for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.